Docket No.: 122.1577 Serial No. 10/759,072

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 1 and 2 and AMEND claims 4, 8, 14, 18, 23, 27, 32, 34, 35, 36, 38, 42, 43, 45 and 47 in accordance with the following:

1. (CANCELLED)

2. (CANCELLED)

3. (CURRENTLY AMENDED) The capacitive load driving circuit as claimed in claim ~~2~~4, wherein said input signal is a positive polarity pulse signal.

4. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim 2~~ A capacitive load driving circuit, comprising:

an input terminal;

a rising edge delay circuit delaying a rising edge of an input signal input via said input terminal;

a falling edge delay circuit delaying a falling edge of said input signal;

an amplifying circuit amplifying a drive control signal obtained through said rising edge delay circuit and said falling edge delay circuit; and

an output switch device driven by said amplifying circuit, wherein:

said rising edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element, and a switch element, and ~~wherein,~~

when said input signal rises, said capacitive element is charged through said resistive element and, when said input signal falls, said capacitive element is discharged through said switch element.

5. (ORIGINAL) The capacitive load driving circuit as claimed in claim 4, wherein said switch element in said rising edge delay circuit is a diode.

6. (ORIGINAL) The capacitive load driving circuit as claimed in claim 4, wherein the delay time of said rising edge delay circuit is adjusted by varying the resistance value of said resistive element.

7. (ORIGINAL) The capacitive load driving circuit as claimed in claim 4, wherein the delay time of said rising edge delay circuit is adjusted by varying the capacitance value of said capacitive element.

8. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim 2~~ A capacitive load driving circuit, comprising:

an input terminal;

a rising edge delay circuit, delaying a rising edge of an input signal input via said input terminal;

a falling edge delay circuit, delaying a falling edge of said input signal;

an amplifying circuit amplifying a drive control signal obtained through said rising edge delay circuit and said falling edge delay circuit; and

an output switch device which is driven by said amplifying circuit, wherein:

said falling edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element, and ~~wherein,~~

when said input signal falls, said capacitive element is charged through said resistive element and, when said input signal rises, said capacitive element is discharged through said switch element.

9. (ORIGINAL) The capacitive load driving circuit as claimed in claim 8, wherein said switch element in said falling edge delay circuit is a diode.

10. (ORIGINAL) The capacitive load driving circuit as claimed in claim 8, wherein the delay time of said falling edge delay circuit is adjusted by varying the resistance value of said resistive element.

11. (ORIGINAL) The capacitive load driving circuit as claimed in claim 8, wherein the delay time of said falling edge delay circuit is adjusted by varying the capacitance value of said capacitive element.

12. (CANCELLED)

13. (CURRENTLY AMENDED) The capacitive load driving circuit as claimed in claim ~~12~~14, wherein said input signal is a negative polarity pulse signal.

14. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim~~ ~~12~~A capacitive load driving circuit, comprising:

an input terminal;

a falling edge delay circuit , delaying a falling edge of an input signal input via said input terminal;

a rising edge delay circuit, delaying a rising edge of said input signal;

an amplifying circuit amplifying a drive control signal obtained through said falling edge delay circuit and said rising-edge delay circuit; and

an output switch device driven by said amplifying circuit, wherein;

said rising edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element, and~~, wherein~~

when said input signal rises, said capacitive element is charged through said resistive element and, when said input signal falls, said capacitive element is discharged through said switch element.

15. (ORIGINAL) The capacitive load driving circuit as claimed in claim 14, wherein said switch element in said rising edge delay circuit is a diode.

16. (ORIGINAL) The capacitive load driving circuit as claimed in claim 14, wherein the delay time of said rising edge delay circuit is adjusted by varying the resistance value of said resistive element.

17. (ORIGINAL) The capacitive load driving circuit as claimed in claim 14, wherein the delay time of said rising edge delay circuit is adjusted by varying the capacitance value of said capacitive element.

18. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim~~ ~~12~~A capacitive load driving circuit, comprising:

an input terminal;

a falling edge delay circuit, delaying a falling edge of an input signal input via said input terminal;

a rising edge delay circuit, delaying a rising edge of said input signal;

an amplifying circuit amplifying a drive control signal obtained through said falling edge delay circuit and said rising edge delay circuit; and

an output switch device which is driven by said amplifying circuit, wherein:

said falling edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element, and ~~wherein,~~

when said input signal falls, said capacitive element is charged through said resistive element, and when said input signal rises, said capacitive element is discharged through said switch element.

19. (ORIGINAL) The capacitive load driving circuit as claimed in claim 18, wherein said switch element in said falling edge delay circuit is a diode.

20. (ORIGINAL) The capacitive load driving circuit as claimed in claim 18, wherein the delay time of said falling edge delay circuit is adjusted by varying the resistance value of said resistive element.

21. (ORIGINAL) The capacitive load driving circuit as claimed in claim 18, wherein the delay time of said falling edge delay circuit is adjusted by varying the capacitance value of said capacitive element.

22. (CANCELLED)

23. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim 1~~A capacitive load driving circuit, comprising:

an input terminal;

a front-edge delay circuit delaying a front edge of an input signal input via said input terminal;

a back-edge delay circuit delaying a back edge of said input signal;

an amplifying circuit amplifying a drive control signal obtained through said front-edge delay circuit and said back-edge delay circuit; and

an output switch device driven by said amplifying circuit, wherein:

said front-edge delay circuit comprises a first capacitive element and a first series circuit having a first resistive element and a first switch element~~; and~~,

said back-edge delay circuit comprises a second capacitive element and a second series circuit having a second resistive element and a second switch element, and~~, wherein~~

said first series circuit and said second series circuit are connected in parallel.

24. (ORIGINAL) The capacitive load driving circuit as claimed in claim 23, wherein said first capacitive element and said second capacitive element are together constructed as one common capacitive element.

25. (ORIGINAL) The capacitive load driving circuit as claimed in claim 23, wherein the delay time of the front edge of said input signal is adjusted by varying the resistance value of said first resistive element, and delay time of the back edge of said input signal is adjusted by varying the resistance value of said second resistive element.

26. (ORIGINAL) The capacitive load driving circuit as claimed in claim 23, wherein said first switch element and said second switch element are diodes.

27. (CURRENTLY AMENDED) A capacitive load driving circuit, comprising:

an input terminal;

a front-edge delay circuit delaying a front edge of an input signal input via said input terminal;

a back-edge delay circuit delaying a back edge of said input signal;

an amplifying circuit amplifying a drive control signal obtained through said front-edge delay circuit and said back-edge delay circuit; and

an output switch device is driven by said amplifying circuit~~The capacitive load driving circuit as claimed in claim 1~~, wherein:

said front-edge delay circuit comprises a first resistive element and a first capacitive element~~; and~~,

said back-edge delay circuit comprises a second capacitive element and a series circuit having a second resistive element and a switch element, and~~, wherein~~

said first resistive element and said series circuit are connected in parallel.

28. (ORIGINAL) The capacitive load driving circuit as claimed in claim 27, wherein said first capacitive element and said second capacitive element are together constructed as one common capacitive element.

29. (ORIGINAL) The capacitive load driving circuit as claimed in claim 27, wherein the delay time of the front edge of said input signal is adjusted by varying the resistance value of said first resistive element, and delay time of the back edge of said input signal is adjusted by varying the resistance value of said second resistive element.

30. (ORIGINAL) The capacitive load driving circuit as claimed in claim 27, wherein the delay time of the front edge of said input signal is adjusted by varying the resistance value of said first resistive element, and thereafter, delay time of the back edge of said input signal is adjusted by varying the resistance value of said second resistive element.

31. (ORIGINAL) The capacitive load driving circuit as claimed in claim 27, wherein said switch element is a diode.

32. (CURRENTLY AMENDED) A capacitive load driving circuit, comprising:

an input terminal;

a front-edge delay circuit delaying a front edge of an input signal input via said input terminal, ~~The capacitive load driving circuit as claimed in claim 1, wherein:~~ said front-edge delay circuit ~~comprises~~ comprising a first counter which starts to count a clock signal from the front edge of said input signal; ~~and~~

a back-edge delay circuit delaying a back edge of said input signal, said back-edge delay circuit ~~comprises~~ comprising a second counter which starts to count said clock signal from the back edge of said input signal~~,~~; ~~and~~

an amplifying circuit for amplifying a drive control signal obtained through said front-edge delay circuit and said back-edge delay circuit; and

an output switch device which is driven by said amplifying circuit, wherein;

~~the~~ a delay time of said front edge is adjusted by varying a count value of said first counter, and

a delay time of said back edge is adjusted by varying a count value of said second counter.

33. (ORIGINAL) The capacitive load driving circuit as claimed in claim 32, wherein said first counter and said second counter are formed on the same semiconductor integrated circuit.

34. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim 1, wherein:~~ A capacitive load driving circuit, comprising:

a first and a second capacitive load driving circuit, each of the first and second capacitive load driving circuits comprising:~~;~~

an input terminal,

a front-edge delay circuit delaying a front edge of an input signal input via said input terminal,

a back-edge delay circuit delaying a back edge of said input signal,

an amplifying circuit amplifying a drive control signal obtained through said front-edge delay circuit and said back-edge delay circuit, and

an output switch device which is driven by said amplifying circuit;

~~said capacitive load driving circuit comprises~~

a first output switch device in said first capacitive load driving circuit ~~is~~ connected between a power line and a capacitive load; and

a second output switch device in said second capacitive load driving circuit ~~is~~ connected between said capacitive load and a reference voltage.

35. (CURRENTLY AMENDED) The capacitive load driving circuit as claimed in claim 34, wherein:

said capacitive load driving circuit further comprises ~~a~~ third and ~~a~~ fourth capacitive load driving circuits;

a third output switch device in said third capacitive load driving circuit is connected to said capacitive load via a first coil; and

a fourth output switch device in said fourth capacitive load driving circuit is connected to said capacitive load via a second coil.

36. (CURRENTLY AMENDED) The capacitive load driving circuit as claimed in claim 34, wherein:

said power supply line is a sustain power supply line of a plasma display apparatus.

37. (CANCELLED)

38. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim 37, wherein:~~A capacitive load driving circuit comprising:

an input terminal;

a front-edge delay circuit ~~said front edge delay circuit comprises~~, comprising a resistive element and a capacitive element, delaying a front edge of an input signal input via said input terminal; ~~and~~

~~said~~ a pulse width adjusting circuit, ~~is~~ comprising a monostable multivibrator, generating a drive control signal having a prescribed pulse width from a delayed signal obtained through said front-edge delay circuit;

an amplifying circuit for amplifying said drive control signal; and

an output switch device which is driven by said amplifying circuit.

39. (ORIGINAL) The capacitive load driving circuit as claimed in claim 38, wherein the delay time of said input signal is adjusted by varying the resistance value of said resistive element in said front-edge delay circuit.

40. (ORIGINAL) The capacitive load driving circuit as claimed in claim 38, wherein the delay time of said input signal is adjusted by varying the capacitance value of said capacitive element in said front-edge delay circuit.

41. (ORIGINAL) The capacitive load driving circuit as claimed in claim 38, wherein the pulse width of said drive control signal is adjusted by varying a time constant and the like of said monostable multivibrator.

42. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim 37, wherein:~~A capacitive load driving circuit, comprising:

~~said~~ a front-edge delay circuit ~~is~~, comprising a first counter ~~for~~ counting a clock signal and delaying a front edge of an input signal input via said input terminal; and

a pulse width adjusting circuit generating a drive control signal having a prescribed pulse width from a delayed signal obtained through said front-edge delay circuit, said pulse width adjusting circuit ~~is~~ comprising a second counter ~~for~~ counting said clock signal, ~~and~~ wherein:

the delay time of said input signal is adjusted by varying a count value of said first counter, and

the pulse width of said drive control signal is adjusted by varying a count value of said second counter~~.~~;

an amplifying circuit amplifying said drive control signal; and

an output switch device driven by said amplifying circuit.

43. (CANCELLED)

44. (CANCELLED)

45. (CANCELLED)

46. (CANCELLED)

47. (CURRENTLY AMENDED) ~~The capacitive load driving circuit as claimed in claim 37, wherein:~~

~~said~~ A capacitive load driving circuit, ~~comprises~~ comprising:

~~a~~ first and ~~a~~ second capacitive load driving circuits, each of the first and second capacitive load driving circuits comprising:~~;~~

an input terminal,

a front-edge delay circuit delaying a front edge of an input signal input via said input terminal,

a pulse width adjusting circuit ~~for~~ generating a drive control signal having a prescribed pulse width from a delayed signal obtained through said front-edge delay circuit,

an amplifying circuit ~~for~~ amplifying said drive control signal, and

an output switch device ~~which is~~ driven by said amplifying circuit;

a first output switch device in said first capacitive load driving circuit ~~is~~ connected between a power line and a capacitive load; and

a second output switch device in said second capacitive load driving circuit ~~is~~ connected between said capacitive load and a reference voltage.

Docket No.: 122.1577 Serial No. 10/759,072

48. (ORIGINAL) The capacitive load driving circuit as claimed in claim 47, wherein:

said capacitive load driving circuit further comprises a third and a fourth capacitive load driving circuit;

a third output switch device in said third capacitive load driving circuit is connected to said capacitive load via a first coil; and

a fourth output switch device in said fourth capacitive load driving circuit is connected to said capacitive load via a second coil.

49. (ORIGINAL) The capacitive load driving circuit as claimed in claim 47, wherein said power supply line is a sustain power supply line of a plasma display apparatus.

50. (CURRENTLY AMENDED) A plasma display apparatus, comprising:

a plurality of X electrodes;

a plurality of Y electrodes which are arranged substantially parallel to said plurality of X electrodes, and which produce a discharge between said plurality of Y electrodes and said plurality of X electrodes;

an X-electrode driving circuit which applies a discharge voltage to said plurality of X electrodes; and

a Y-electrode driving circuit which applies a discharge voltage to said plurality of Y electrodes, and wherein said X-electrode driving circuit or said Y-electrode driving circuit is constructed using a capacitive load driving circuit~~, wherein said capacitive load driving circuit comprises:~~

~~an input terminal;~~

~~a front-edge delay circuit for delaying a front edge of an input signal input via said input terminal;~~

~~a back-edge delay circuit for delaying a back edge of said input signal;~~

~~an amplifying circuit for amplifying a drive control signal obtained through said front-edge delay circuit and said back-edge delay circuit; and~~

~~an output switch device which is driven by said amplifying circuit~~as recited in any of claims 4, 8, 14, 18, 23, 27, 32, 34, 38, 42 and 47.

51. (CURRENTLY AMENDED) A plasma display apparatus, comprising:

a plurality of X electrodes;

a plurality of Y electrodes which are arranged substantially parallel to said plurality of X electrodes, and which produce a discharge between said plurality of Y electrodes and said plurality of X electrodes;

an X-electrode driving circuit which applies a discharge voltage to said plurality of X electrodes; and

a Y-electrode driving circuit which applies a discharge voltage to said plurality of Y electrodes, and wherein said X-electrode driving circuit or said Y-electrode driving circuit is constructed using a capacitive load driving circuit as recited in any of claims 4, 8, 14, 18, 23, 27, 32, 34, 38, 42, and 47, ~~wherein said capacitive load driving circuit comprises:~~

~~an input terminal;~~

~~a front-edge delay circuit for delaying a front edge of an input signal input via said input terminal;~~

~~a pulse width adjusting circuit for generating a drive control signal having a prescribed pulse width from a delayed signal obtained through said front-edge delay circuit;~~

~~an amplifying circuit for amplifying said drive control signal; and~~

~~an output switch device which is driven by said amplifying circuit.~~